of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

a second insulating film formed on said first electrode layer and said element isolating region, an open portion exposing a surface of said first electrode layer being formed in said second insulating film; and

a second electrode layer formed on said second insulating film and said exposed surface of said first electrode layer, said second electrode layer being electrically connected to said first electrode layer via said open portion, said first and second electrode layers including a gate electrode, said open portion having a first width in a direction of a gate length of said gate electrode and a second width in a direction perpendicular to the direction of the gate length, the second width being greater than the first width.

3. (Amended) The semiconductor device according to claim 1, wherein said gate electrode is a gate electrode of a selective transistor included in a NAND type flash memory.

5. (Amended) The semiconductor device according to claim 1, which is a semiconductor device in a memory cell array region, comprising:

said semiconductor layer;

said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating film;

said element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

said second insulating film formed on said first electrode layer and said element isolating region; and

[1] A marked-up copy of the changes made to the claims is attached.

said second electrode layer formed on said second insulating film;

wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

32. (Amended) The semiconductor device according to claim 1, wherein an electric resistance of said second electrode layer is lower than that of said first electrode layer, and said second electrode layer comprises a metal layer including a high melting point or a lamination layer film comprising a metal silicide layer including a high melting point and a polysilicon layer.

34. (Amended) The semiconductor device according to claim 1, wherein said second insulating film comprises a complex insulating film including a silicon nitride film.

36. (Amended) The semiconductor device according to claim 1, which is a semiconductor device in which said second insulating film remains at an edge portion of said gate electrode.

Please add new Claims 61 and 62 as follows:

61. (New) The semiconductor device according to claim 1, wherein said open portion extends over element regions identical to said element region, in the direction perpendicular to the length of the gate length.

62. (New) The semiconductor device according to claim 61, wherein said element isolating insulating film is provided between said element regions, and includes a groove formed in said element isolating insulating film, and said groove is located under said open portion, and has a same shape as said open portion.